* NOTICES *

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3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The drain field which consists of a semi-conductor of the first conductivity type, and the insulated gate laid under the slot dug deep by the front face of this drain field at U typeface, In the electrostatic-induction semiconductor device equipped with the source field of the first conductivity type by which was formed in the front face of said drain field, and ohmic contact was carried out to the source electrode The electrostatic-induction semiconductor device characterized by having the contact field of the second conductivity type by which was formed in the front face of said drain field, and touched the insulator layer of said insulated gate, and ohmic contact was carried out to said source electrode.
[Claim 2] The drain field which consists of a semi-conductor of the first conductivity type, and the insulated gate laid under the slot dug deep by the front face of this drain field at U typeface, In the electrostatic-induction semiconductor device equipped with the source field of the first conductivity type by which was formed in contact with said drain field, and ohmic contact was carried out to the source electrode The electrostatic-induction semiconductor device characterized by for said a part of drain field [at least] contacting said source electrode directly, and forming the Schottky barrier in these contact surfaces.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to an insulated-gate mold electrostatic-induction semiconductor device.
[0002]
[Description of the Prior Art] The gate of many of electrostatic-induction semiconductor devices, such as a static induction transistor (SIT) currently made available from the former, was a junction gate. However, the electrostatic-induction semiconductor device using a junction gate has the problem that the consumed electric current at the time of a turn-off is large, it is the purpose of gate drive power reduction, and the electrostatic-induction semiconductor device of a format using the insulated gate is proposed (JP,55-99774,A).
[0003] Drawing 13 is drawing showing an example of the electrostatic-induction semiconductor device of the insulated-gate mold indicated by JP,55-99774,A, and is the sectional view showing the electrostatic-induction thyristor which carries out bipolar actuation. In drawing 13 , 1 is n-mold drain field, 2 is p+ mold drain field, and n+ mold drain field 3 intervenes between these n-mold drain field 1 and p+ mold drain field 2. 4 is the drain electrode formed in contact with p+ mold drain field 2 on the rear face of a semiconductor device. It is the gate electrode with which 5 was formed in gate dielectric film and 6 was formed on this gate dielectric film 5. It is the source electrode with which 7 was formed in n+ mold source field, and 8 was formed on n+ mold source field 7, and this n+ mold source field 7 is formed in the front face of n-mold drain field 1. In the example shown in drawing 13 , a slot is formed in n-mold drain field 1 between each n+ mold source field 7, and gate dielectric film 5 is formed in the inside of this slot.
[0004] Next, actuation of this equipment is explained. It sets to drawing 13 and an electrical potential difference forward in touch-down and the drain electrode 4 is impressed to the source electrode 8. If a negative predetermined electrical potential difference is impressed to the gate electrode 6, a depletion layer will be formed in n-mold drain field 1 of the n+ mold source field 7 circumference, the current path between n+ mold source field 7 and p+ mold drain field 2 will be intercepted, and a thyristor will be turned off. On the other hand, if an electrical potential difference is not impressed to the gate electrode 6 or a forward electrical potential difference is impressed to it, the depletion layer which was being developed around n+ mold source field 7 will be lost, and a thyristor will be turned on.
[0005] In addition, in the example shown in drawing 13 , it has the function which prevents that a depletion layer develops to p+ mold drain field 2 in n-mold drain field 1 where high impurity concentration is low, and n+ mold drain field 3 produces a punch-through phenomenon, and controls the minority carrier injection from p+ mold drain field 2 to n-mold drain field 1.
[0006]
[Problem(s) to be Solved by the Invention] However, in the electrostatic-induction semiconductor device of the conventional insulated-gate mold mentioned above, in the ON state, a lot of minority carriers are poured into n-mold drain field 1 of the gate-dielectric-film 5 circumference from p+ mold

drain field 2, and n-mold drain field 1 of this gate-dielectric-film 5 circumference has equipment in a high level impregnation condition.
[0007] Although it is possible to be able to reduce the carrier consistency in a drain field for a short time, and to shorten time amount by the turn-off by drawing out directly a lot of minority carriers which exist around the gate from a gate electrode in the electrostatic-induction semiconductor device of a junction-gate mold In the electrostatic-induction semiconductor device of an insulated-gate mold For this reason, since a lot of minority carriers which exist around this insulated gate 5 through the insulated gate 5 cannot be missed, and there is no place to go to of these minority carriers, it cannot but wait for a minority carrier to carry out natural disappearance in n-mold drain field 1. Therefore, in the electrostatic-induction semiconductor device of an insulated-gate mold, the time amount by the turn-off was taken for a long time, and there was a problem of leading to the loss of power consumption.
[0008] Moreover, also in a static OFF state, when the high voltage was impressed to a drain electrode, the inversion layer was formed around this gate dielectric film 7 of the minority carrier opposite-generated within the depletion layer of the gate-dielectric-film 7 circumference, and there was also a problem that there was a possibility that a drain electrical potential difference may be built over gate dielectric film 7, without extending a depletion layer, and gate dielectric film 7 may be destroyed. This phenomenon may be similarly generated in the static induction transistor of the unipolar actuation which the drain field 2 becomes from n+ mold field.
[0009] the purpose of this invention is made in order to solve the trouble of the above conventional techniques -- having -- base -- it is in offering the electrostatic-induction semiconductor device [a quick turn-off is possible and] which can moreover protect gate dielectric film from an excessive drain electrical potential difference at the time of cutoff.
[0010]
[Means for Solving the Problem] If it matches and explains to drawing 1 and drawing 11 which show one example, this invention will be applied to the electrostatic-induction semiconductor device equipped with the drain field 11 which consists of a semi-conductor of the first conductivity type, the insulated gate (14 15) laid under the slot dug deep by the front face of this drain field 11 at U typeface, and the source field 17 of the first conductivity type by which was formed in the front face of said drain field 11, and ohmic contact was carried out to the source electrode 19. And invention of claim 1 has attained the above-mentioned purpose by touching said insulated gate (14 15) and forming in the front face of said drain field 11 the contact field 18 of the second conductivity type by which ohmic contact was carried out to said source electrode 19. Moreover, invention of claim 2 has attained the above-mentioned purpose by contacting said a part of drain field [at least] 11 to said source electrode 19 directly, and forming the Schottky barrier 25 in these contact surfaces.
[0011]
[Function] The inversion layer formed in the about 14 gate dielectric film drain field 11 in the cut off state of an electrostatic-induction semiconductor device is connected to the source electrode 19 through the contact field 18 or the Schottky barrier 25 formed in the front face of this drain field 11. Therefore, the potential of this inversion layer is always being fixed to the same potential as the source electrode 19. Moreover, when it faces across the field 12 of the second conductivity type between the drain field 11 and the drain electrode 13 in order to carry out bipolar actuation, A lot of minority carriers which exist in the about 17 source field drain field 11 at the time of the turn-off which shifts to a cut off state from a conductivity modulation condition It flows into the source electrode 19 through the contact field 18 or the Schottky barrier 25 of drain field 11 front face through an about 14 gate dielectric film [which occurs with the negative electrical potential difference impressed to the gate electrode 15 that it should make a cut off state] inversion layer. for this reason, the about 17 source field drain field 11 depletion-izes promptly -- having -- base -- a quick turn-off is realized.
[0012] In addition, although drawing of an example was used by the term of above-mentioned The means for solving a technical problem explaining the configuration of this invention, and an operation in order to make this invention intelligible, thereby, this invention is not limited to an example.
[0013]

[Example] - 1st example- drawing 1 is the sectional view showing the electrostatic-induction thyristor which is the 1st example of the electrostatic-induction semiconductor device by this invention. In drawing 1 , 11 is n-mold drain field, 12 is p+ mold drain field, and the drain electrode 13 is formed in the rear face of this p+ mold drain field 12.
[0014] Two or more slots which have a perpendicular field along the depth direction of this n-mold drain field 11 are formed in the front face of n-mold drain field 11, and gate dielectric film 14 is formed in the inside of these slots. Moreover, the gate electrode with which 15 was formed in this gate dielectric film 14, and 16 are the interlayer insulation films formed in the front face of the gate electrode 15. Therefore, the insulated gate of the thyristor of this example has composition laid under the front face of n-mold drain field 11. The insulated gate is constituted by the gate electrode 15 and gate dielectric film 14.
[0015] 17 is n+ mold source field formed in the front face of n-mold drain field 11 which corresponds between phase next door **** gate dielectric film 14. 18 is p+ mold contact field formed in the front face of n-mold drain field 11 which corresponds between these n+ mold source field 17 and gate dielectric film 14. This n+ mold source field 17 and gate dielectric film 14 consist of this examples so that it may not touch directly and may touch through p+ mold contact field 18.
[0016] 19 is a source electrode, and this source electrode 19 is formed so that the front face of all n+ mold source fields 17 and p+ mold contact fields 18 may be touched.
[0017] The high impurity concentration of n+ form source field 17 is set as three or more [5x1019cm -] values, and ohmic contact is carried out to the source electrode 19. Moreover, ohmic contact also of the p+ mold contact field 18 is carried out to the source electrode 19. In addition, in the following explanation, n-mold drain field 11 across which it faced between phase next door **** gate dielectric film 14 is called "channel field" 20 of the semiconductor device of this example, the depth from H and n+ mold source field 17 pars basilaris ossis occipitalis to gate electrode 15 pars basilaris ossis occipitalis is set to L for the distance between phase next door **** gate dielectric film 14, and this distance L is called "channel length" of the semiconductor device of this example.
[0018] Next, actuation of the electrostatic-induction thyristor of this example is explained. The source electrode 19 is grounded first and a forward electrical potential difference is impressed to the drain electrode 13. And in order to make a thyristor into an OFF state, a negative low battery is impressed to the gate electrode 15. By setting the gate electrode 15 as low negative potential, a depletion layer is formed in n-mold drain field 11 of the gate-dielectric-film 14 circumference, this depletion layer depletion-izes the above-mentioned channel field 20, the current path between n+ mold source field 17 and p+ mold drain field 13 is intercepted, and a thyristor is turned off.
[0019] Under the present circumstances, although the inversion layer by the electron hole is formed in the front face of the gate dielectric film 14 with which a depletion layer exists, since this inversion layer is in contact with p+ mold contact field 18 in the front face of n-mold drain field 11, the potentials of an inversion layer are this p+ mold contact field 18 as a result the source electrode 19, and this potential, and are held uniformly. Therefore, the electrical potential difference which should be impressed to the gate electrode 15 mentioned above does not need to impress the excessive negative electrical potential difference beyond it that what is necessary is just a negative electrical potential difference required in order that potential may form the inversion layer held uniformly.
[0020] Next, in order to carry out the turn-on of the thyristor, a forward electrical potential difference is impressed to the gate electrode 15, it replaces with the inversion layer by the electron hole, and the accumulation layer by the electron is formed around gate-dielectric-film 14. Thereby, the conduction electron from n+ mold source field 17 flows from the pars basilaris ossis occipitalis of this gate dielectric film 14 to n-mold drain field 11 through the accumulation layer of the gate-dielectric-film 14 circumference, and a thyristor is turned on. For this reason, most drift resistance of the channel field 20 in an ON state becomes small to extent which can be disregarded.
[0021] thus, if a thyristor will be in an ON state and conduction electron is emitted to n-mold drain field 11 from n+ mold source field 17, an electron hole will be emitted to n-mold drain field 11 also from p+ mold drain field 12, this n-mold drain field 11 will be in a high level impregnation condition,

conductivity modulation will be carried out and it will fall [resistivity will be markedly alike and].
[0022] Furthermore, in order to carry out the turn-off of the thyristor, a negative low battery is again impressed to a gate electrode, it replaces with the accumulation layer by the electron, and the inversion layer by the electron hole is formed around gate-dielectric-film 14. Immediately after impressing a negative electrical potential difference, n-mold drain field 11 is in a high level impregnation condition, and many electron holes exist in n-mold drain field 11 of the n+ mold source field 17 circumference. However, since this field is in contact also with p+ mold contact field 18 and an electron hole flows promptly to the source electrode 19 through an about 14 gate dielectric film inversion layer and p+ mold contact field 18, the high level impregnation condition in n-mold drain field 11 of the n+ mold source field 17 circumference is canceled promptly. By this, a depletion layer is formed in the channel field 20, the current path between p+ mold drain field 13 and n+ mold source field 17 is intercepted, and a thyristor is turned off.
[0023] Next, the conditions of the distance H between gate dielectric film 14 are explained. Certain conditions are required in order to intercept the current path in this thyristor, when the thyristor of this example is an OFF state. B-B' in drawing 1 to which drawing 2 met in the direction which intersects perpendicularly with channel length L -- it is drawing showing the energy band in the field of a between. In drawing 2 , the band shown in right-hand side by separating is the thing of p+ mold contact field 18 fixed to the source electrode 19 and this potential, and the potential of gate dielectric film 14 is in agreement with this band. Moreover, the broken line of the center of each band shows the location of a mid gap, and Eg is bandgap energy.
[0024] In order to intercept a current path, the channel field 20 must be depletion-ized completely. That is, as shown in drawing 2 (a), only as for Eg/2, in the core of the channel field 20, the potential of a conducting sleeve lower limit must turn up at least from Fermi level EF of n+ mold source field 17. Since this field cannot be completely depletion-ized if a part lower than Eg/2 is in the potential of the conducting sleeve lower limit in the channel field 20 as shown in drawing 2 (b), the remarkable leakage current flows the channel field 20, and cutoff of a current path is not fully attained.
[0025] The distance H between the gate dielectric film 14 for satisfying the cutoff conditions shown in drawing 2 (a) is expressed with the conditions of a degree type.
[Equation 1]

$$\frac{q \cdot N_D}{2 \cdot \varepsilon si} \left(\frac{H}{2}\right)^2 < \phi_{P^+}$$

here -- q -- base -- a charge and Np are the donor concentration of the channel field 20, and the potential of the mid gap about which epsilonSi measured the dielectric constant of silicon, and phip+ from the Fermi level in p+ mold contact field 18. As an example, if Np=5x1014cm-3 and phip+=0.56eV, it will be set to H= (abbreviation) 2.47 micrometers. It can be said that the numeric value of this H will not very be an advanced technique if it carries out from a current photo etching technique.
[0026] Furthermore, the conditions of channel length L are explained. When using the electrostatic-induction thyristor of this example as the so-called component of a pentode property, it must be desirable for the side face of the insulated gate which faces across the channel field 20 to be perpendicular as much as possible to the front face of a component, and the still more nearly certain conditions also about channel length L must be satisfied.
[0027] Even if the channel field 20 is depletion-ized by the electric field by the insulated gate, potential is bent in the about 18 n+ mold source field channel field 20 by the effect of this n+ mold source field 18. It is clear by numerical calculation (simulation) that this effectiveness reaches in the direction of channel length L (that is, perpendicular direction) to the Hth place of distance about. Such a phenomenon happens similarly about the channel field 20 of the part (that is, near gate-dielectric-film 14 pars basilaris ossis occipitalis) near p+ mold drain field 12.
[0028] That is, the side attachment wall of the insulated gate which faces across the channel field 20 is formed in a vertical plane, the range where the effect by the range and n+ mold source field 18 to which

the effect of drain electric field will reach if a drain electrical potential difference becomes [L/H] high or less by two reaches [the distance H between gate dielectric film 14] the place which this channel field 20 reaches in a fixed case is connected, and the current-voltage characteristic of a component turns into a triode property. On the contrary, about with [L/H] two [or more], however high a drain electrical potential difference may become, the range where the effect of drain electric field reaches is not connected with the range where the effect by n+ mold source field 18 reaches, and the current-voltage characteristic of a component turns into a pentode property. Although the critical value of these triodes property and a pentode property becomes settled according to the high impurity concentration and geometric structure of the channel field 20, for realizing the component of a pentode property, it requires that L/H is three or more as a realistic value.

[0029] The range where the effect according to drain electric field as compared with the case where the side attachment wall of the insulated gate is formed in the vertical plane if the side attachment wall of the insulated gate is not formed in a vertical plane as shown in drawing 3 , but it takes beyond at the pars basilaris ossis occipitalis of the insulated gate, and the distance H between gate dielectric film 14 becomes large, namely, it is formed in breadth at last reaches spreads even in the channel field 20 interior further. As shown in drawing 3 , in order to realize the component of H1, then a pentode property for the distance between gate dielectric film [in / for the distance between the gate dielectric film 14 in the edge by the side of the source field 18 of the channel field 20 / the edge by the side of H0 and the drain field 12] 14, the conditions of L>H0+H1 must be satisfied.

[0030] Thus, in order to realize the component of a pentode property, it is desirable for the side attachment wall of the insulated gate which faces across the channel field 20 to be perpendicular as much as possible to the front face of a component, and he can understand that the still more nearly certain conditions (L/H> as a realistic value 3) also about channel length L must be satisfied.

[0031] The above electrostatic-induction thyristors of a configuration are manufactured according to the process shown in drawing 4 - drawing 8 as an example. First, as shown in drawing 4 , n-mold epitaxial layer (drain field) 11 which has given thickness and predetermined high impurity concentration on p+ mold substrate (drain field) 12 is grown up. While a side attachment wall forms a slot field almost perpendicular to the front face of n-mold epitaxial layer 11 in the front face of this n-mold epitaxial layer 11 and forming gate dielectric film 14 in the inside of this slot field By forming the gate electrode 15 in this gate dielectric film 14, and forming an interlayer insulation film 16 in that front face, the insulated gate is laid underground in a slot field.

[0032] Next, as shown in drawing 5 , only a depth of thousands of A removes the front face of n-mold epitaxial layers 11 other than the insulated gate by etching, and the ion implantation of the impurity for p+ mold contact field 18 formation is carried out to the etched front face.

[0033] Next, as shown in drawing 6 , the sidewall section 21 which turns into the side-attachment-wall section of the gate dielectric film 14 exposed by etching and an interlayer insulation film 16 from Si3N4 is formed. That thickness deposits Si3N4 about 5000A uniform film on the whole front face of etched n-mold epitaxial layer 11 everywhere, and this sidewall section 21 is formed by removing by anisotropic etching.

[0034] Furthermore, as shown in drawing 7 , after only a depth of about 2000A removes the front face of n-mold drain field 11 by etching by using the sidewall section 21 as a mask, the ion implantation of the impurity for n+ mold source field 17 formation is carried out.

[0035] And as shown in drawing 8 , about 2000A of Si3N4 film 22 is deposited on a front face, into nitrogen-gas-atmosphere mind, the impurity which performed and carried out the ion implantation of 1000 degrees C and the annealing for about 20 minutes is activated, and n+ mold source field 17 and p+ mold contact field 18 are formed. Then, if a heat phosphoric acid removes Si3N4 surface film 22 and the source electrode 19 is formed in a front face, the electrostatic-induction thyristor of structure as shown in drawing 1 can be obtained.

[0036] As explained above, to the electrostatic-induction thyristor of this example Since p+ mold contact field 18 adjacent to the both sides of gate dielectric film 14 and the source electrode 19 is formed The electron hole of a large number which exist in about 17 n+ mold source field n-mold drain field 11

at the time of a turn-off an about 14 gate dielectric film inversion layer and p+ mold contact field 18 -- minding -- the source electrode 19 -- it can pass -- base -- a quick turn-off can be realized and reduction of power consumption can be aimed at. Moreover, since the inversion layer formed in about 14 gate dielectric film in a static OFF state is also in contact with this p+ mold contact field 18, the potential of an inversion layer is fixed to the same potential as the potential of p+ mold contact field 18, as a result the source electrode 19. Thereby, even when the high voltage is impressed to a drain electrode, the electrical potential difference concerning gate dielectric film 14 is held uniformly, and the situation of the electrostatic discharge of an insulator layer 14 like before can be avoided.

[0037] - Modification of the 1st example - In contact [by the part] in the 1st above-mentioned example, although n+ mold source field 17 and the side face of gate dielectric film 14 do not touch directly. That is, predetermined spacing is set in the boundary section of n+ mold source field 17 and gate dielectric film 14, p+ mold contact field 18 is formed in it, and you may make it gate dielectric film 14 touch it p+ mold contact field 18, n+ mold source field 17, and by turns, as shown in drawing 9 . Thus, the fall of on resistance can be aimed at by contacting a part of n+ mold source field 17 on the side face of gate dielectric film 14.

[0038] - 2nd example- drawing 10 is the sectional view showing the electrostatic-induction thyristor which is the 2nd example of the electrostatic-induction semiconductor device by this invention. In addition, in the following explanation, the sign same about the same component as the 1st above-mentioned example is attached, and the explanation is simplified.

[0039] In this example, p+ mold drain field 12 and the drain electrode 13 are formed in the front face of the same side as the source electrode 19, and n+ mold drain field 23 and the drain electrode 24 are formed in the background of n-mold drain field 11.

[0040] Therefore, also by this example, the electrostatic-induction thyristor which performs the same actuation as the 1st above-mentioned example can be realized, and the same effectiveness can be acquired. Especially, in this example, when a drain electrical potential difference is below a build in (interior) electrical potential difference between n-mold drain field 11 and p+ mold drain field 12 (about 0.6 V), the current path of the n+ mold drain field 23 ->n-mold drain field 11 ->n+ mold source field 18 is secured, and there is an advantage that the rise of on resistance can be controlled, by performing unipolar actuation.

[0041] - 3rd example- drawing 11 is the sectional view showing the electrostatic-induction thyristor which is the 3rd example of the electrostatic-induction semiconductor device by this invention. In this example, it replaces with p+ mold contact field 20 in the 1st above-mentioned example, n-mold drain field 11 and the source electrode 19 are contacted directly, and the Schottky barrier 25 is formed among these. Therefore, the same operation effectiveness as the 1st above-mentioned example can be acquired also by this example.

[0042] - 4th example- drawing 11 is the sectional view showing the static induction transistor which is the 4th example of the electrostatic-induction semiconductor device by this invention. In this example, it replaces with p+ mold drain field 12 in the 1st above-mentioned example, and n+ mold drain field 26 is formed in the background of n-mold drain field 11. Therefore, the same operation effectiveness as the 1st above-mentioned example can be acquired also by this example. Since especially the static induction transistor of this example performs unipolar actuation, in an ON state, conductivity modulation of the n-mold drain field 11 is not carried out, but there is an advantage that the time amount by the turn-off is quick.

[0043] In addition, the details are not limited to each above-mentioned example, but various modifications are possible for the electrostatic-induction semiconductor device of this invention.

[0044]

[Effect of the Invention] As explained to the detail above, according to invention of claim 1, the contact field of an electric conduction form contrary to a source field adjacent to the both sides of gate dielectric film and a source electrode was prepared. Moreover, according to invention of claim 2, a part of drain field [at least] forms the Schottky barrier directly in contact with a source electrode. pass the inversion layer near the gate dielectric film in a lot of minority carriers which exist in the drain field near the

source field by this at the time of a turn-off -- a contact field or the Schottky barrier -- minding -- a source electrode -- it can pass -- base -- a quick turn-off can be realized and reduction of power consumption can be aimed at. Moreover, since the inversion layer formed near the gate dielectric film in a static OFF state is also in contact with this contact field or Schottky barrier, the potential of an inversion layer is fixed to the same potential as a source electrode. The electrical potential difference concerning gate dielectric film is held uniformly by this, and the situation of the electrostatic discharge of an insulator layer like before can be avoided.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view showing the electrostatic-induction thyristor which is the 1st example of the electrostatic-induction semiconductor device by this invention.
[Drawing 2] It is drawing for explaining the conditions of the distance between gate dielectric film.
[Drawing 3] It is drawing for explaining channel length's conditions.
[Drawing 4] It is process drawing for explaining the manufacture approach of the electrostatic-induction thyristor of the 1st example.
[Drawing 5] It is the same drawing as drawing 2 .
[Drawing 6] It is the same drawing as drawing 3 .
[Drawing 7] It is the same drawing as drawing 4 .
[Drawing 8] It is the same drawing as drawing 5 .
[Drawing 9] It is drawing showing the modification of the 1st example, and is the view sectional view which meets the A-A'line of drawing 1 .
[Drawing 10] It is the sectional view showing the electrostatic-induction thyristor which is the 2nd example of the electrostatic-induction semiconductor device by this invention.
[Drawing 11] It is the sectional view showing the electrostatic-induction thyristor which is the 3rd example of the electrostatic-induction semiconductor device by this invention.
[Drawing 12] It is the sectional view showing the static induction transistor which is the 4th example of the electrostatic-induction semiconductor device by this invention.
[Drawing 13] It is the sectional view showing an example of the conventional electrostatic-induction thyristor.
[Description of Notations]
11 N-Mold Drain Field
12 P+ Mold Drain Field
13 24 Drain electrode
14 Gate Dielectric Film
15 Gate Electrode
17 N+ Mold Source Field
18 P+ Mold Contact Field
19 Source Electrode
20 Channel Field
23 26 n+ mold drain field
25 Schottky Barrier

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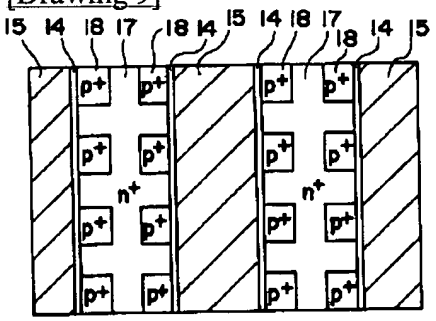
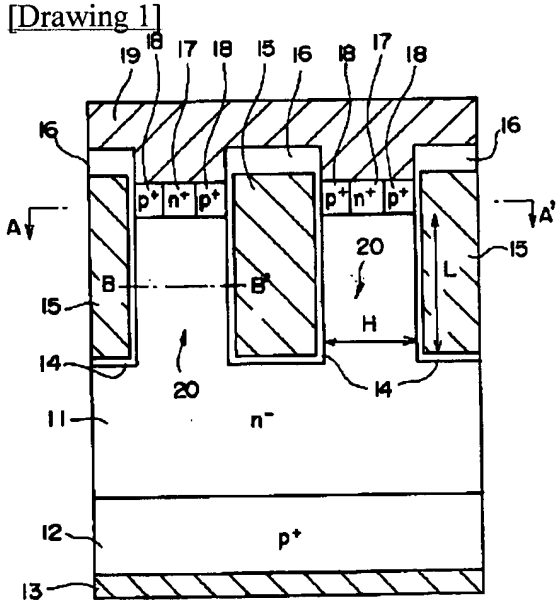
DRAWINGS

[Drawing 9]

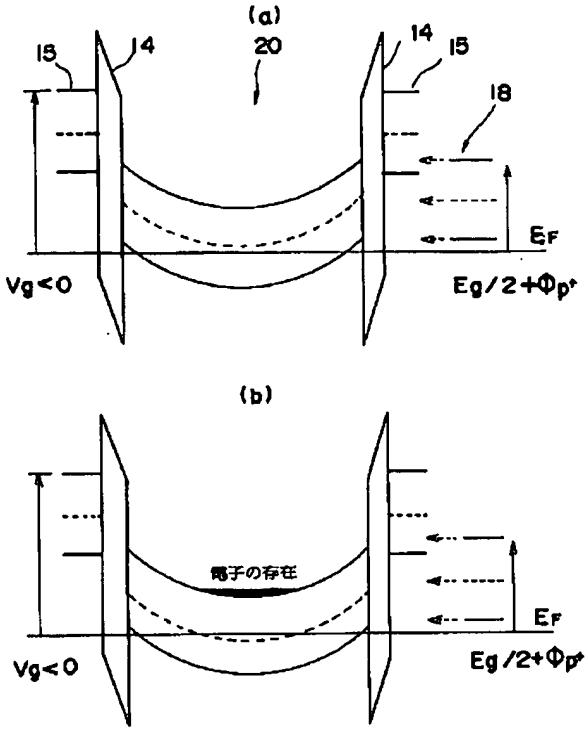


[Drawing 1]

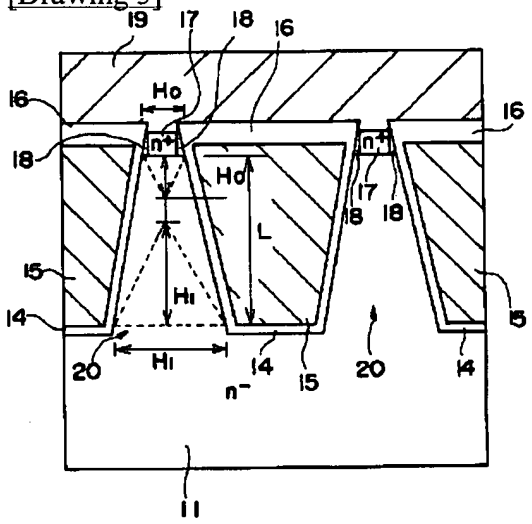


11：n⁻型ドレイン領域　17：n⁺型ソース領域
13：ドレイン電極　18：p⁺型コンタクト領域
14：ゲート酸化膜　19：ソース電極
15：ゲート電極　20：チャネル領域

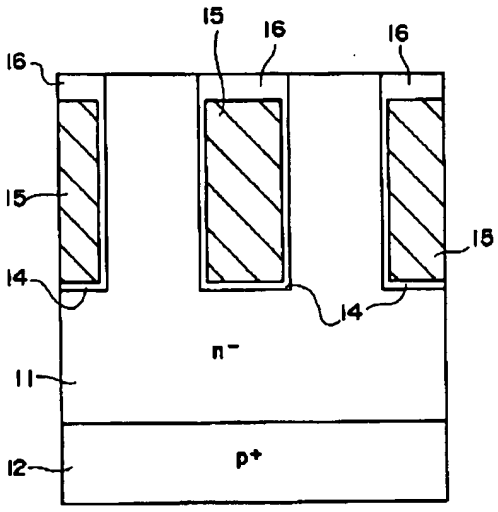
[Drawing 2]



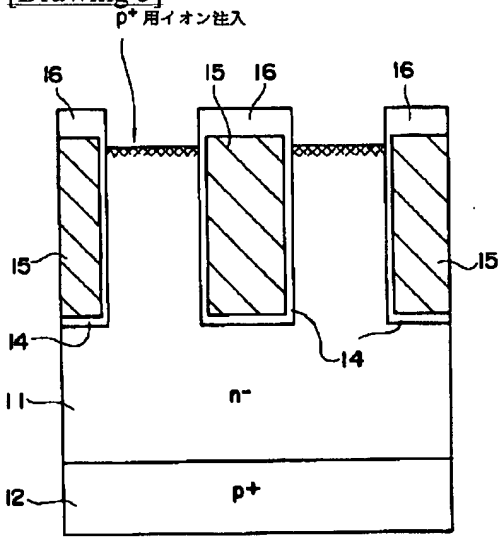
[Drawing 3]



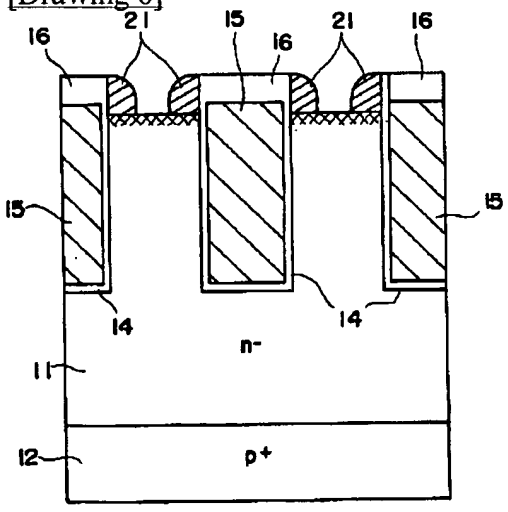
[Drawing 4]



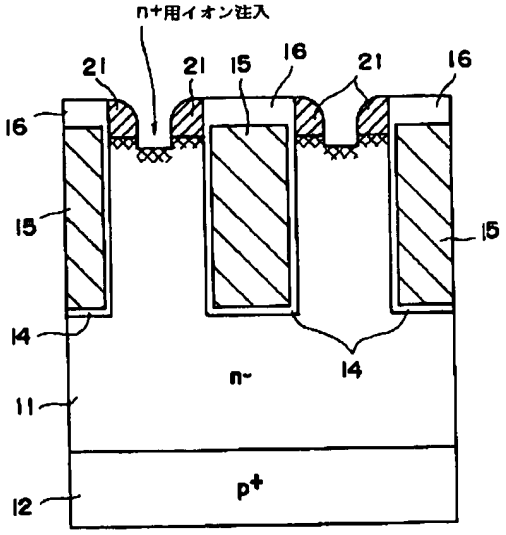
[Drawing 5]



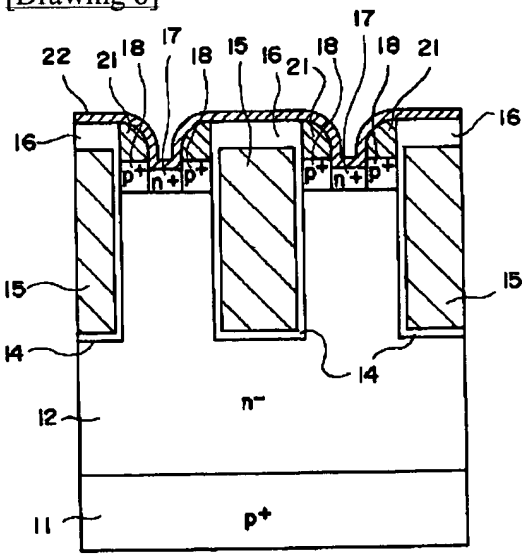
[Drawing 6]



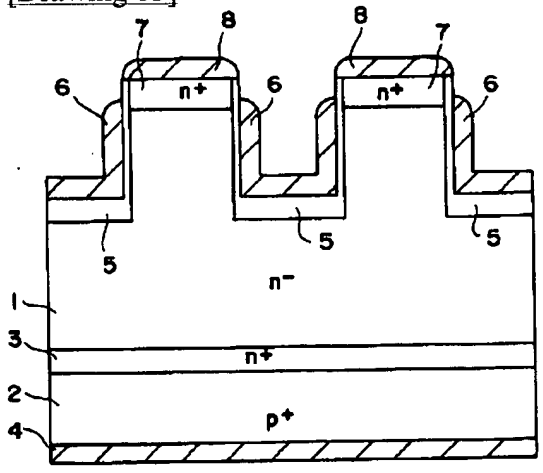
[Drawing 7]



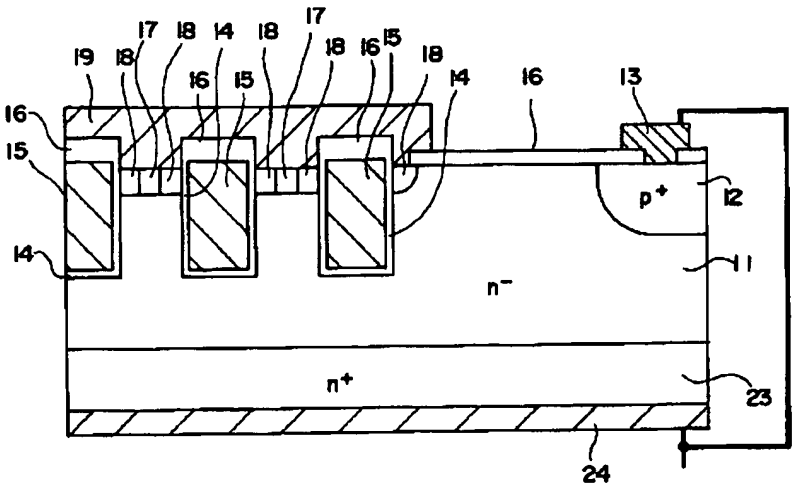
[Drawing 8]



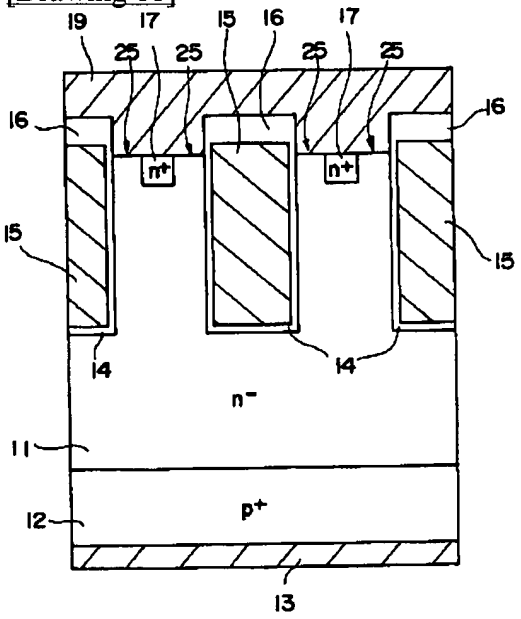
[Drawing 13]



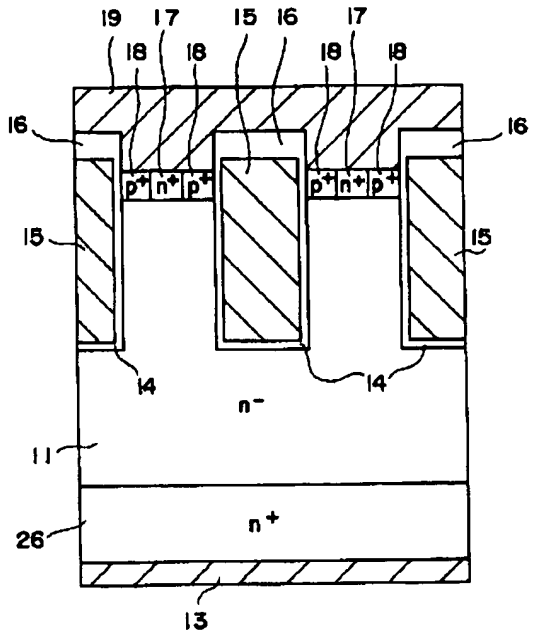
[Drawing 10]



[Drawing 11]



[Drawing 12]



[Translation done.]